CLAIMS

What is claimed is:

1. An apparatus comprising:

a processor interface unit; and

a cache to store information received from a processor coupled to the processor interface unit, the cache to store disposable information.

2. The apparatus of claim 1, the cache to further store non-disposable information.

3. The apparatus of claim 2, further comprising a cache management unit to determine whether a cache entry contains disposable information.

4. The apparatus of claim 3, further comprising a bus interface unit to allow a device coupled to the bus interface unit to access the cache.

5. The apparatus of claim 4, the cache management unit to allow the cache entry to be overwritten if the device coupled to the bus interface unit reads the cache entry and if the cache management logic determines that the cache entry contains disposable information.

6. The apparatus of claim 5, further comprising a system memory controller.

7. The apparatus of claim 6, the cache management unit to cause the cache entry contents to be delivered to the system memory controller for delivery to a system memory if the cache management unit determines that the cache entry does not contain disposable information.

8. The apparatus of claim 7, the processor interface unit to receive a disposable information attribute indication from the processor when the processor delivers disposable information to the processor interface unit.

9. The apparatus of claim 7, the cache management unit to determine whether the cache entry contains disposable data by comparing the cache entry address with a range of addresses that define a disposable information address space.

10. The apparatus of claim 9, further comprising at least one programmable register to store addresses that define a disposable address space.

11. A system, comprising:

a processor; and

a system logic device coupled to the processor, the system logic device including

a processor interface unit, and

a cache to store information received from a processor coupled to the processor interface unit, the cache to store disposable information.

12. The system of claim 11, the cache to further store non-disposable information.

13. The system of claim 12, the system logic device further including a cache management unit to determine whether a cache entry contains disposable information.

14. The system of claim 13, the system logic device further including a bus interface unit.

15. The system of claim 14, further comprising a device coupled to the system logic device bus interface unit.

16. The system of claim 15, the cache management unit to allow the cache entry to be overwritten if the device coupled to the bus interface unit reads the cache entry and if the cache management logic determines that the cache entry contains disposable information.

17. The system of claim 16, the system logic device further including a system memory controller.

18. The system of claim 17, further comprising a system memory coupled to the system memory controller.

19. The system of claim 18, the cache management unit to cause the cache entry contents to be delivered to the system memory controller for delivery to the system memory if the cache management unit determines that the cache entry does not contain disposable information.

20. The system of claim 19, the processor interface unit to receive a disposable information attribute indication from the processor when the processor delivers disposable information to the processor interface unit.

21. The system of claim 19, the cache management unit to determine whether the cache entry contains disposable data by comparing the cache entry address with a range of addresses that define a disposable information address space.

22. The system of claim 21, the system logic device further including at least one programmable register to store addresses that define a disposable address space.

23. A method, comprising:

receiving a line of information from a processor;

storing the line of information in a cache;

determining whether the line of information is disposable; and

writing the line of information to a system memory if the information is not disposable.

24. The method of claim 23, further comprising allowing the line of information to be overwritten without first writing the line of information to the system memory if the line of information is disposable and if the line of information has been read by a system device.

25. The method of claim 24, wherein determining whether the line of information is disposable includes examining an attribute communicated along with the line of information by the processor.

26. The method of claim 24, wherein determining whether the line of information is disposable includes comparing the address of the line of information with a range of addresses that defines a disposable information address space.